High voltage IC design and development considerations

Introduction:

This paper is a distillation of what we have learnt while designing high voltage analog integrated circuits using processes from well known and established fabrication houses.

Discussion:

- Our high voltage experience has been primarily gained in BiCMOS high voltage technology from two vendors. The salient features of the processes are:
- Both bipolar and MOS transistors available on the same substrate
- Twin voltage capability: 5V and 55V to 450V
- Other elements such as resistors, capacitors, multiple metal interconnect also available.
- Currents of the order of 6 Amp peak for very small durations driving primarily capacitive loads.

Breakdown voltages/punchthrough voltages:

In high voltage design these voltages play a crucial role both for functionality and for reliability. The following discussion focuses first on the breakdown voltages for bipolars and then on the breakdown/punchthrough voltages for MOSFETs.

BVCBO and BVCEO: BVCBO is the *collector to base breakdown* voltage of the common emitter bipolar with the base floating. BVCEO is the *collector to emitter breakdown voltage* with the base open. The two are related through the following:

$$BVCEO = BVCBO(1/HFE)^{1/n} \qquad (1)$$

Where n = 4 for npn and 2 for pnp silicon transistors.

If the base is not open circuited then assume that the base is returned to the emitter through a resistor RB. Then the collector to emitter voltage breakdown voltage is given by BVCER. BVCER lies somewhere in between BVCEO and BVCBO.
To estimate BVCER the following simplifying assumptions are made:

(A) Before the threshold voltage of the bipolar junction is reached, all the current flows through the base and through the resistor RB.

(B) When the threshold voltage is exceeded all the additional current flows through the emitter junction and the corresponding breakdown voltage is BVCEO.

Then,

$$BVCER = BVCBO[1-(ICORB/Vt)]^{1/n} \quad (2)$$

Where ICO is the reverse collector to base current. (Which should be very small).

When the base is short circuited to the emitter the breakdown voltage is denoted by BVCES. The equation above suggests that BVCES = BVCBO. This would be the case if there was absolutely no resistance between base and emitter.

However, we must remember that there is a small base spreading resistance always present between base and emitter. Therefore the total base to emitter resistance should be RB + rbb'. Here rbb' is the base spreading resistance. The upshot is that the voltage BVCES is always less than BVCBO.

After breakdown occurs, the collector and the emitter currents will become very large in comparison to the base current. Therefore at large currents the presence of the base resistor RB makes no difference and the voltage across the bipolar drops to BVCEO from BVCER.

The breakdown voltage BVCER may be increased by returning the resistor RB to some other voltage VBB which keeps the base emitter junction reverse biased.

In this case the condition that determines the onset of breakdown is when the reverse collector current flowing through the resistor RB causes a voltage drop of Vt + VBB.

In this case the breakdown voltage is represented by BVCEX given by:

$$BVCEX = BVCBO[1 - \{ ICO(RB + rbb')/(Vt + VBB)\}]^{1/n} \quad (4)$$

MOSFETs have similar breakdown voltages in their drain and source junctions where junction breakdown occurs. However they also have additional "breakdown" voltages. These are the punchthrough voltage and the gate oxide breakdown voltage.

Punchthrough voltages: Since the drain of a MOSFET and the bulk operates in reverse bias, there is always a depletion layer present at the drain. As the drain – source voltage is increased this depletion layer starts spreading towards the source.

When it reaches the source the MOSFET is said to be in *punchthrough* and the drain source current can no longer be controlled by the gate.

Another issue of MOSFET breakdown is the breakdown voltage of the gate oxide. There is a tradeoff between the gate oxide thickness, the gain of the MOSFET and the gate oxide breakdown voltage.

If the voltage between the gate and the bulk, or the voltage from the gate to the source exceeds the critical oxide breakdown voltage the gate oxide breaks down and burns. The transistor becomes non operational.

In order to keep the gain high, the gate oxide has to be kept thin. If the gate oxide is thin is breaks down at lower voltages. Thus in high voltage MOSFET processes careful trade offs are made in these quantities.

The processes that we have worked with generate both thin oxide high voltage MOSFETs and thick oxide high voltage MOSFETs.

As can be expected the thin oxide high voltage MOSFET has a high drain to source voltage breakdown but a *low* gate to source and gate to bulk breakdown (~ 5.0V for a 55V VDS breakdown transistor).

The thick oxide transistor has a high gate to source and gate to bulk breakdown (~ 20V for 55V VDS breakdown) but much lower gain.

Safe Operating Area: For all these active devices the process technology defines safe operating areas or SOA. This simply ends up being an inverse relationship between various voltages.

For example for the high voltage thin oxide MOSFET quoted above , it is possible to have a drain to source voltage of 50V but the gate to source can only be 5.0V It is important to follow the guidelines for the SOA if catastrophic failure of the device is to be avoided or for good reliable operation.

Surface Inversion: One of the effects that are not so important in low voltage design is the case of inversion of substrate areas. For example a metal line running between two diffusions (unrelated) can turn into a gate turning ON the parasitic MOSFET made by the unrelated diffusions (they need to be of the same type) and the metal which acts as a gate.

These parasitic effects abound in high voltage design and should be taken seriously or else when the power is first switched on the chip will latch solidly causing the power supply to crowbar! Unfortunately most layout verification programs cannot really detect these types of situations easily and thus added effort in CAD may become necessary.

Noise: Note that if there are high voltage switching waveforms on the chip, these will be excellent sources of noise. Noise can couple to sensitive nodes in a variety of ways.

The most important coupling mechanisms are interconnect coupling and substrate coupling. Interconnect lines lying close together with one line being connected to a sensitive input while the other has a high voltage switching waveform on it is a perfect case of trouble!!

In this case the lines should be isolated with a metallic shield in the same level of interconnect as the noisy conductors and connected to a relatively low noise ground. Another case might be an interconnect line running over a gate conductor. All these effects must be taken care of.

Substrate noise is coupled to every device if the process is junction isolated. All devices are situated in the substrate therefore noise in the substrate can couple to every device from every device unless care is taken to isolate sensitive devices with guard rings (diffusions whose width determines isolation efficacy) connected to appropriate power or ground.

Device Models: High voltage device models are more complicated. The high voltage effects need to be modeled carefully otherwise non-modeled parasitic devices associated with all HV devices can cause a lot of problems.

Layout: In general high voltage devices will be larger in size in layout than low voltage devices. Therefore *expect layouts of high voltage chips to be large* and the chip size will also be larger. This of course has an impact on cost. The spacing between active devices must be larger and there must be a guard bands. This also adds to the overall size increase. Metallic interconnect may need to have rounded corners specially for really high voltage design (> 100V). Layout verification is more difficult since standard CAD packages do not have all the options necessary for checking high voltage layout. The layout of high voltage devices is an art and much more complicated than low voltage layout. In fact for the very high voltage devices it may need several iterations of device design and fabrication/characterization to generate safe layout. The design ramification is that flexibility is lost. Random device layout can no longer be done. The actual high voltage standard cells provided by the process vendor must be used *as is* and any changes will cause problems.
