What is load pull analysis for power amplifiers and how is it done?

1.0 Definition:

Load pull analysis is used to construct a set of contours (typically on a Smith Chart), which determine the maximum power output achievable with a given load impedance. These contours are very useful in assessing the actual impedance a device should see when it is used in an amplifier.

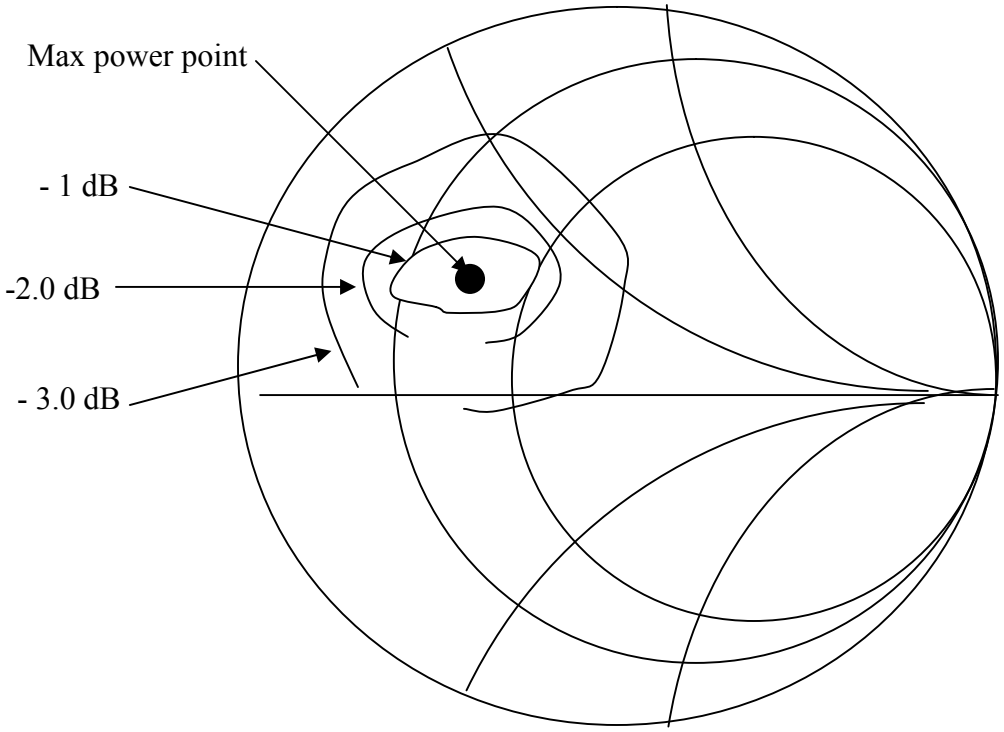

Figure 1.0. Load pull contours

The contours are constructed in the following way:

The device or amplifier under test (DUT) operates between two impedances, one at the input and one at the output. Between these impedances sit two tuners, an input tuner and an output tuner.

The function of the input tuner is to adjust the matching such that the large signal input power is always a constant, even when the output impedance and the output tuner is adjusted.

Initially the closest match at the output is found for the optimum output impedance (See earlier article about load lines and impedances). This is done by adjusting both the input and the output tuners to get the maximum constant output power. This forms the center of the load pull loci *and is a single impedance.*

Next the output impedances are changed and the input tuner is adjusted to provide conjugate matching and thus constant input power. This is repeated as many times as possible and for each constant output power point, a set of loci are generated which provide the impedances which provide that power. These loci are shown on Smith Chart above.

Note that each contour represents the maximum output power achievable with a given load impedance. Load pull contours are useful in determining the actual impedance a device should see when used in an amplifier.

They also predict graphically what will happen when the load changes from the optimum load due to any anomalies such as aging and other variations in the impedances at the output and is a valuable aid in the design and evaluation of power amplifiers.

A precautionary step needs to be taken however. Load pull tuners can accurately synthesize a given load impedance; this impedance is only at a known fundamental frequency. Unfortunately, the harmonic impedances that result from particular settings of the tuners are usually not characterized.

The harmonic impedances can make a significant difference to the efficiency of the device , so load pull characterization needs to be carefully interpreted if contours of constant efficiency are measured instead of constant output power.

If the device is not heavily saturated then the error of changing harmonic terminations between open and short circuits is usually less than a dB or so.

2.0 Analytical Treatment of load pull.

Load pull analysis can be attempted analytically. It starts by using the the expression for the load impedance at the internal nodes of the transistor for maximum linear power just at the 1 dB compression point.

$$ROL = 2VDD/IMAX \qquad (1.0)$$

VDD = Supply voltage
IMAX = Maximum current
ROL = Optimum load impedance for maximum linear power.

Obviously this defines the output power contour for the maximum power and it becomes a point on the load pull contours shown above.

When the load impedance is less than ROL, then the power becomes dependent on the maximum current swing. This is because when ZL (the output impedance) is smaller than the ROL, more current is required to generate a large voltage swing and hence more power. This is the case of current limited power.

When the load impedance is larger than ROL, then power becomes dependent on the voltage swing of the device since a larger voltage swing is required to generate the a large current and hence a large output power. This is the case of voltage limited power.

Note that in each of the above cases the input power is assumed to be sufficient to still drive the device to a maximum current or a maximum voltage.

The input power is continuously tuned to keep it constant.

In the case of current limited power, the load impedance ZL = RL + jXL is being driven. The maximum linear power an then be written as:

$$PO = (1/2)IPEAK^2 * RL \qquad (2.0)$$

The peak to peak output voltage is:

$$ABS(VPP) = IMAX*SQRT(RL^2 + XL^2) \quad (3.0)$$

Using equation 1.0,

$$IMAX = 2VDD/ROL \quad (4.0)$$

Then,

$$ABS(VPP) = (2VDD/ROL)* SQRT(RL^2 + XL^2) \quad (5.0)$$

Now, in case of a current limited amplifier, the voltage swing never gets to the maximum 2VDD, then the following must be true:

For ABS(VPP) = 2VDD,

We must have,

$$SQRT(RL^2 + XL^2) /(ROL) = 1 \quad (6)$$

Or,

$$RL^2 + XL^2 = ROL^2 \quad (7)$$

So for,

$$ABS(VPP) < 2VDD$$

We must have,

$$ROL^2 = RL^2 + XL^2$$

Or,

$$ABS(XL^2) \leqq ROL^2 - RL^2 \quad (8)$$

Looking at the voltage limited case, a dual analysis can be done. In this case it is appropriate to use a parallel admittance,

$$YL = GL + jB \qquad (9)$$

In this case, a dual analysis yields the maximum linear power,

$$PO = (1/2)*VPEAK^2 / RL$$
$$= (1/2)(VDD)^2*GL \qquad (10)$$

In an analogous manner to the development for the current limited case, In the voltage limited case the current never gets to its full output swing. Therefore the susceptance must follow the expression given below:

$$ABS(BL) \leqq (GOL^2 - GL^2) \qquad (11)$$

From these equations one can derive load pull power contours as follows:

A: Determine the optimum load impedance ROL from equation (1). This provides the maximum power point (the center of the load pull contours)

B: Generate the ratio of the given power level PO with respect to optimum power POPT (as above in A:) Then,

$$PO/POPT = RL/ROL \text{ (for current limited case)}$$

Or

$$PO/POPT = GL/GOL$$

For the voltage limited case.

C: Using the ratios of power above determine the resistive points on the contour of that power level. To clarify this further, if the ratio of the current limited case for the power levels is 0.7, then RL = 0.7ROL. This provides the resistive point for starting the construction of the contour.

Starting at the *smaller resistance* the contour follows a constant resistance line on the Smith Chart up to the *reactance limits* given by equation 8.

If starting at *a higher resistance,* the contour follows a *constant conductance* line on the Smith Chart up to the susceptance limits given by equation 11.0

D: Finally move the reference plane from the interior or intrinsic side of the device to the external device terminals and include device output shunt capacitance and bondwire parasitics into the measurement.

This then provides a procedure to allow load pull contours to be generated by hand. The are a number of CAD tools today that can do this and if such a tool is available by all means it should be used. However, the engineer should know a priori approximately what to expect otherwise the process will not be a closed one for how does the engineer know if the CAD tool result is near or accurate?