Manchester decoder

Manchester Code

Manchester code embeds clock information with data in a very simple way: each bit is transmitted with a transition in the middle of the bit time. For a '0', transition is 0 to 1, for a '1', transition is 1 to 0 (Figure 1).

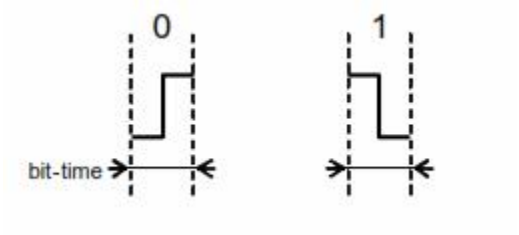

Figure 1.0 Manchester encoding protocol

Figure 2.0 below illustrates a manchester encoded bit stream.

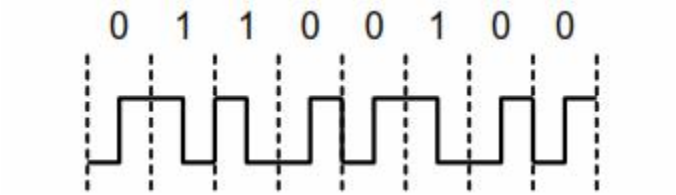

Figure 2.0 Multiple bits in manchester format

The idea is to have multiple transitions in the stream even for long sequences of '1' and '0' data. This enables the manchester data stream to carry the clock as well as the data. The data and clock can be extracted by a manchester decoder, the subject of this brief article.

The principle of the decoder presented in this article.

Note, from Figure 2.0 above, that the bit value is present during the first half of bit time, before the

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transition edge. If a delay of *three-fourths bit time* is triggered by the incoming mid-bit transition, the value captured at the end of the delay will indicate the next bit value. Please see Figure 3.0 below.

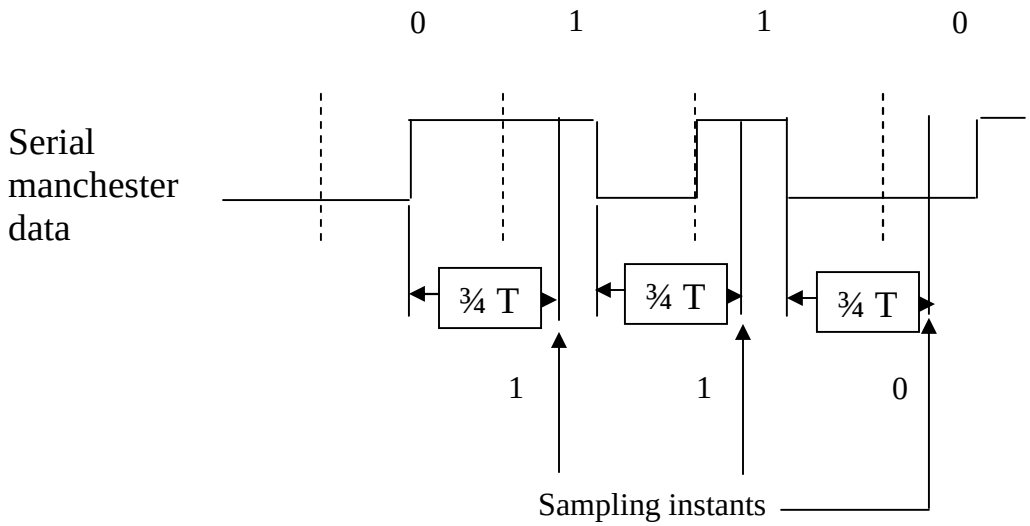

Figure 3.0 Principle of the decoder

If the next bit value is ‘1’, the receiver sets a signal to invert the input bit stream polarity, so the next signal transition appears as a low-to-high transition (Figure 4). If the next bit value is ‘0’, the receiver resets the inverted signal.

The figure below shows this operation graphically.

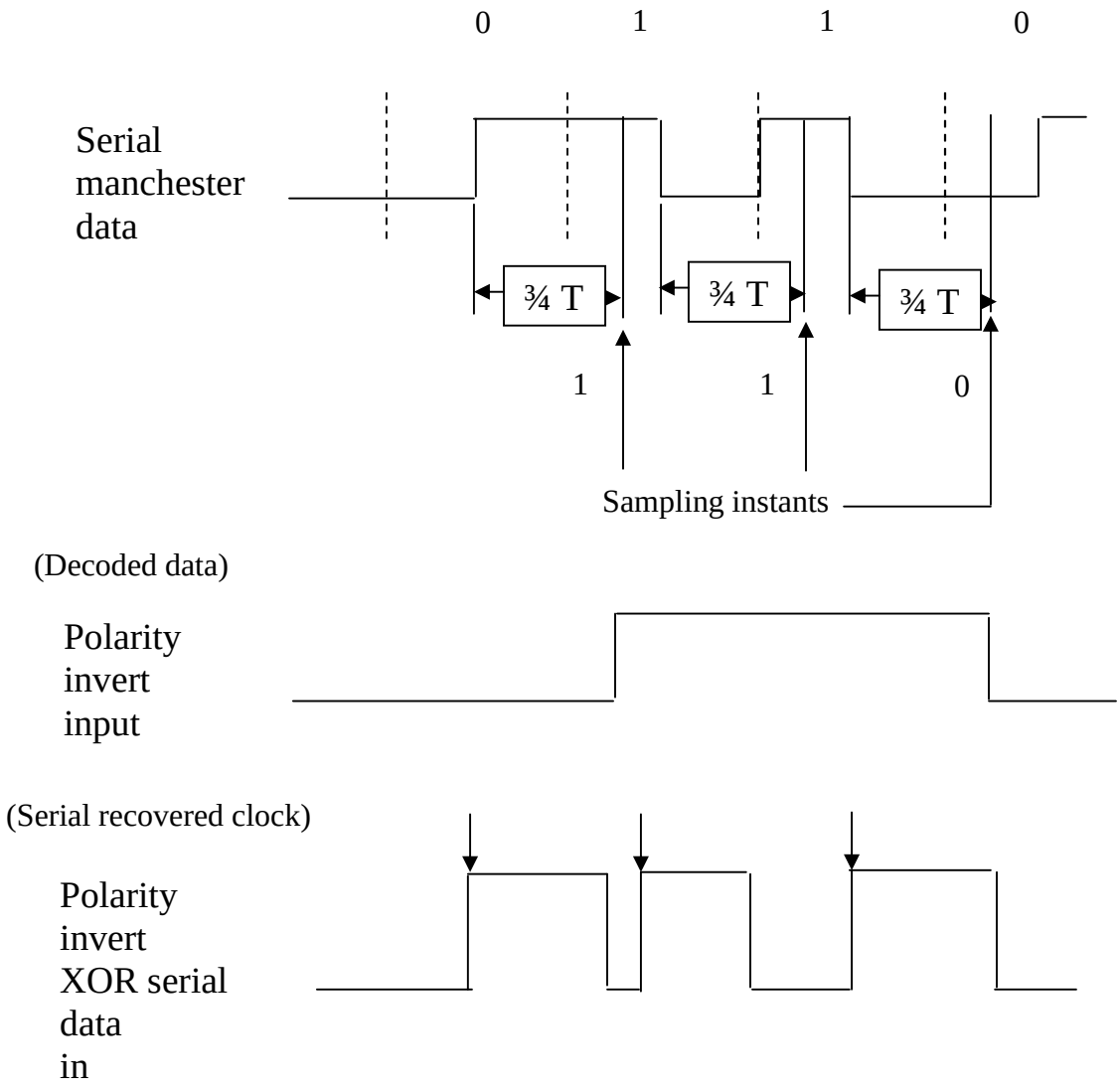

Figure 4.0 Principle of the receiver

This fundamental operation is embodied in the schematic shown below

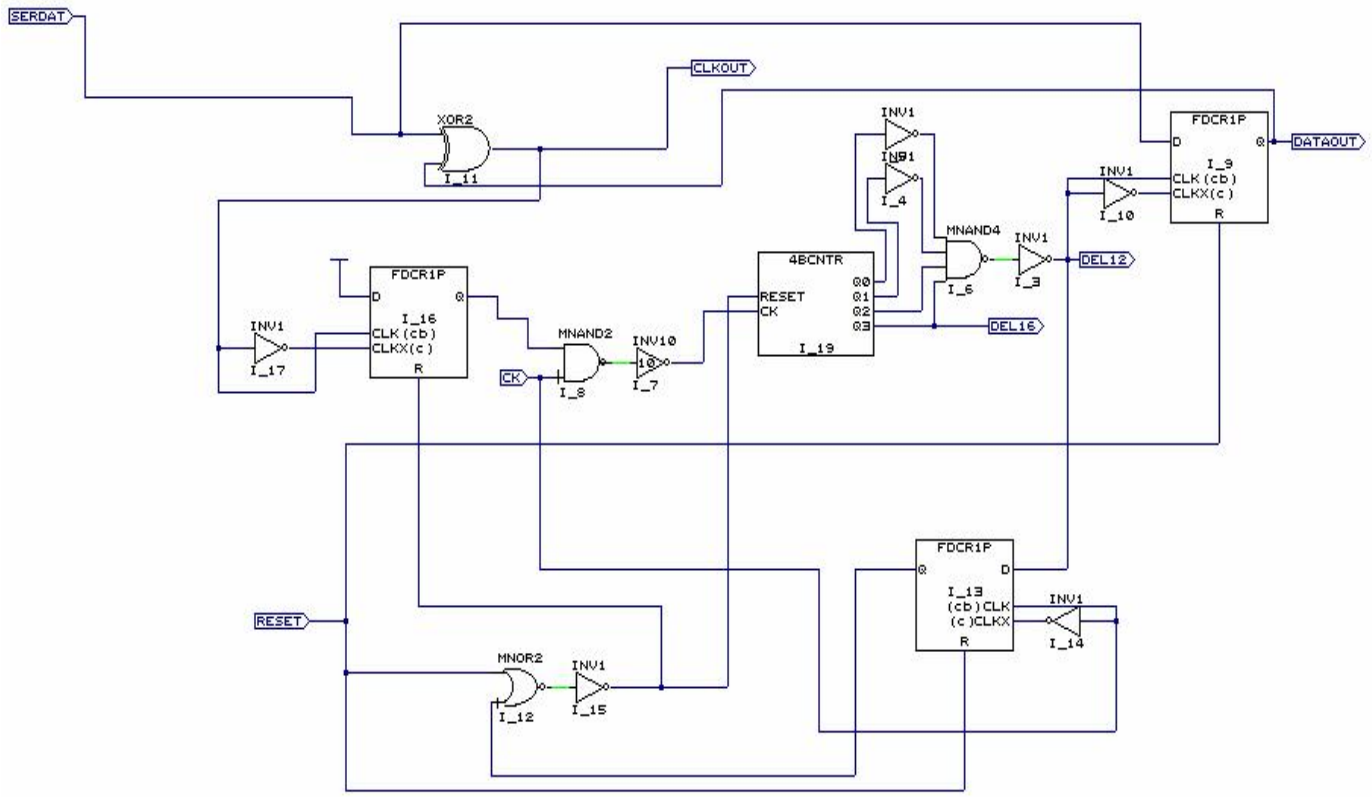

Figure 5: The receiver

A 16X bit rate clock is used. A 4 bit counter follows the clock. A decoding circuit is used at the output of the counter to generate a ¾ period delay (DEL12). The positive edge of this signal is used as the clock input of the following DFF. Each time this positive edge occurs the value (1 or 0) at the D input of the FF is captured.

The output of this FF is connected to one input of the XOR gate. The other input of the XOR is connected to the serial data input. The falling edge of the XOR starts the operation by allowing the clock to be gated to the counter. The DEL12 output resets the operation automatically. An external

hard reset is provided at the Reset input also, that sets all the variables to their initial states for correct operation.

Using this schematic as a reference and the description of the decoder presented above it should be clear that this circuit implements the operation accurately.

Any questions or comments should be referred to the author via email: spg@signalpro.biz or spg327@gmail.com.