Technical Memorandum and Program Plan for the Project

- Prepared by: SPG Staff, Signal Processing Group, Chandler, Arizona

Introduction: After a fairly detailed discussion on the requirements of this project while we were visiting with the customer, we have come up with the following assessments on the project needs, techniques and constraints. We have also in this discussion attempted to provide a budgetary plan for execution of the project that can be used as a preliminary quotation if necessary. A timeline is also outlined.

Technical Discussion: The chip itself is basically a tranceiver, which acts a data pipe for transmit, receive, clock recovery , encoding and decoding (CODEC function) and data buffering. Some of the circuitry on the chip is high speed digital. The analog content of the chip is associated with clock recovery and synchronization which is done via a Phase and frequency locked loop.

I will start with the PLL. The PLL will be a second order PLL (Type II). This loop consists of a VCO, a binary divider (/N), a Phase/Frequency detector and supporting analog and digital circuitry composed of op amps, current sources, voltage sources, voltage references and combinational and sequential logic machines. The PLL function is to regenerate the clock at the receiving end, and synchronize this clock to the received signal enabling the data to be extracted.

Most of the PLL circuitry is contained on the chip. The external components will consist of the loop filter, which consists of 2 capacitances (of the order of nF) and one resistor.

There will also be a need for random logic and at least one state machine on the chip. There will also be a need for FIFOs to buffer the data stream at both ends and also a simple uP interface.

Apart from the PLL these will all be digital circuits.

From an assessment of the frequencies, voltage levels and impedances my recommendation is, that we use a standard double poly, double metal, 0.8um CMOS process to implement the entire chip. If we find that 0.8um is not sufficiently fast (for the clocks and the PLL) we can easily transition to a 0.6um version of the process with minimal disruption. This decision I think should be made after we have had time to design and simulate the circuit. In any case our operating supply voltage should not exceed 6.0V if we are to take advantage of the high performance of these processes. We believe that this the case in the present design. The cost factor between these processes is not a great concern since the very first lot of wafers should yield all the die that the project needs for sampling. Production issues have not been addressed in the development plan.

The number of pins on the chip, apart from being dictated by the operational I/O of the device will also be conditioned by the need to prevent noise and jitter of the PLL. From

our earlier assessments (in the cafeteria, no less) we know we don't have a lot of slop in the operation of the PLL. To understand this effect consider what will happen when a 40Mhz per volt VCO is operated in the presence of noise. A one volt control voltage swings the VCO by 40Mhz. The 40 Mhz may actually be a reasonable Kv for our application. Therefore the jitter per millivolt may be as much as 40 kHz. Considerations such as these prompt us to propose multiple supply and ground pins for the device as well as due considerations for bypassing the supply. In addition let us also make provision for ferrite beads on the supply lines (just in case). Additionally, while we are on the subject let us make sure we understand the importance of the board or substrate layout.

For the actual design of the PLL we will be using techniques we have used during the past few years and therefore hope for low risk.

Finally to end this short discussion of technical assessments we strongly advocate the use of test chips (low cost prototyping) to check out the operation of various critical parts of the chip even before the final chip is fabricated. We will make this part of the program plan. This procedure will not delay the chip by any means, however its impact will be felt in the reduction of risk and a slight increase in cost. This extra expense in my opinion is well worth the money.

I also want to point out that this effort will involve a significant amount of close work between the team at SPG and the team at the customer's site. We will propose that we work out the methodology of data exchange (i.e. schematics, verilog/VHDL files, simulation results, reviews, telephonic conference calls, travel, etc) at a fairly early date. As is well known, lack of clear, timely and detailed communication accounts for 95% of failures in projects of this kind. I am assuming, correctly I am sure, that customer's engineers are the experts in the subsystem we are proposing to integrate, while we at SPG provide expert assistance to them to use semiconductor technology/substrate to integrate their design. This forms the fundamental tenet of our belief.

Program Plan: Before we start on the main body of the program plan, we would like to make a disclaimer. This plan is based on what we consider realistic expectations. It is neither optimistic nor pessimistic. In other words this plan is not something we can tweak and trim to our hearts content and yet hope for success.

In addition we must all be aware, right off the bat, that ICs of this nature do not work the first time to specifications or even to functional levels. Although all precautions are taken to ensure (and to target a first pass success) it wiser to expect that the first silicon will probably not work completely. Parts of it will work very well but by the same token there may be parts of it that don't work at all. Therefore this plan will call for test chips and debugging techniques to make sure that we do not need too many iterations. We always assume that we will need one full mask set fabrication, one more with maybe 2 or 3 masks modified and perhaps one final iteration with a single mask to completely bring the operation of the chip into a full specification compliance mode. To expect anything

better than this would be very optimistic. The techniques and tools that we as a team (i.e. the customer team and SPG team) will have at our disposal to avoid major disasters are the following (in our opinion. We may be able to add others):

1.0 Definition: Let us work closely together to make sure we define the device /external components/substrate in as much detail as we can and as accurately as we can. If we are unsure of any spec. or function , make it a candidate for a test chip or pre-production chip. Let us spend some time to make a good specification that *is completely and thoroughly understood* by all parties. Make sure this is fully documented and signed off. Changes to the specification are not a problem as long as all of us understand the ramifications. These include schedule and budget increases. Any items that drop into a crack at this stage will cause us much grief, therefore again we stress the need for communications. Fortunately today we do have access to fast and written communications so this should not be a problem as long as we start with the attitude that allows us to communicate freely and frequently. I recommend at least a couple of trips so that face to face meetings may be held at least to finalize things and once in between.

2.0 Communications: We need to establish close communications so that day to day work on the project can be smoothly coordinated. We can do this via any of the methods below:

Phone: SPG phone number (602)892-1399
Conference call facilities available by calling
Maria Sala at SPG.

FAX: SPG FAX number (602)892-1782

e-mail for SPG (general): spg@goodnet.com
sigproc@primenet.com

Mohammad's direct e –mail: mafo@worldnet.att.net

Mohammad's cell phone: (602)999-8567

Graphics or text can be sent over e-mail using the Adobe Acrobat Exchange. We will set up our schematics capture package with the customer team so that we can exchange schematics over e-mail.

Logic simulation results can be sent using the Adobe Acrobat Exchange format. Analog simulation results can be sent either using the Adobe Acrobat Exchange format or if the customer team has Microsim PSPICE in the form of .cir, .OUT and .DAT files.

Layouts can be viewed by using the layout viewers which we will set up at the customer's premises.

We use both Word 7 (Microsoft Word) and WordPerfect 5.1 for our alpha documentation. We should standardize on one of these formats.

We need to review what work we have done on a weekly conference call for minor milestones and face to face for major milestones. I think reviews are a must and we should take them seriously.

3.0 Documentation: We should take the time to document everything that is of any significance at all. Specifically all schematics should be documented, all simulation results should be documented, all changes should be documented, all articles of specifications should be documented. All out of date items should be archived and removed from active working areas as soon as agreement is reached that these are old items. All correspondence should be documented. e – mails of course are self documenting but we should make sure we don't erase any of these as they may be useful in the course of the project. All layout databases will be documented and the above comments on old databases will be applicable.

4.0 Methodology: The methodology for the execution of the project is one the best tools we have ensure success and to track the project. In this memorandum I have used a program plan as a good substitute for methodology i.e. read methodology for program plan. This plan is of course open to modification by the Customer. After some modifications we should agree on the methodology and execute accordingly.

Methodology is also very important in one other aspect. The methodology also defines a set of expectations both for the customer and SPG. In other words a task is defined, a deliverable is defined and a set of conditions for the acceptance of the deliverable is defined. For the customer this means that the definition of what " done" means is defined while for SPG in addition to defining what "done" means, it defines the payment milestone. There should be no arguments about payment or successful completion of a task. Lack of such an expectation list is the leading cause of friction between a customer and a vendor and we want to avoid this situation like the plague. We will touch on the payment issue later on in the financial issues section.

Program Plan: This program plan tabulates the tasks to be done, an estimated time frame in Working Weeks (WW), a result or deliverable to be generated and an estimated investment. For the purposes of this program plan all tasks will be deemed to be done in series. Obviously, there is always an option to do some tasks in parallel and this will be obvious from the context. The idea is to lay out the various tasks so that we don't overlook some critical issue which will get us later on.

Task 1: Definition: Define chip functions, I/O, timing diagrams, numerical specifications, min, typ, max values, system interface, external components, board level interactions and parasitics and document all.

Time: (Add for particular project)
Deliverables: Document Rev 1.0, signed off.
Investment: (Add for particular project)

Task 2: Technology Parameters: Obtain all the process parameters, design rules, choose the foundry, setup agreements with fabs, packaging facilities etc.

Time: (Add for particular project)
Deliverables: Documents on all design rules, process parameters, electrical parameters, agreements, etc.
Investment: (Add for particular project)

Task 3: Setup Design System: Capture all process parameters in run files for simulations. Set up layout (Mask Design) technology files including set up for Design Rule Checks, netlist Extraction from layout, layout to Schematic verification etc.

Time: (Add for particular project)
Deliverables: All files and documentation
Investment: (Add for particular project)

Task 4: Partition entire chip into appropriate functional blocks and define all interfaces between blocks and methods of simulation appropriate for each function and its interface.

Time: (Add for particular project)
Deliverables: Block diagrams and interface specifications
Investment: (Add for particular project)

Task 5: Design and simulate each functional block with appropriate interface loading Factors, both internal and external.

Time: (Add for particular project)
Deliverables: Schematics and simulation results
Investments: (Add for particular project)

Task 6: Simulate major portions of the complete chip, i.e. combine the appropriate functional blocks and resimulate to check operation with pads, external components, external parasitics, PCB interface.

Time: (Add for particular project)
Deliverables: Schematics and simulation results
Investments: (Add for particular project)

Task 7: Layout the functional blocks of the chip.

Time:	(Add for particular project)
Deliverables:	Layout database, layout verification results
Investment:	(Add for particular project)

Task 8: Layout the test chip with all functional blocks and any other test structures. Note, this will be a superset of the final chip. Do DRC, LVS and any other verification which will reduce risk. Prepare for test chip fabrication.

[Notes: This step does increase the investment. However, it is up to you to judge whether a reduction in risk is worth the effort and investment.]

Time:	(Add for particular project)
Deliverables:	Complete test chip database with verification results.
Investment:	(Add for particular project)

Task 9: Send the test chip for low cost fabrication.

Time:	(Add for particular project)
Deliverables:	Packaged samples of test chip [10 or so]
Investments:	(Fab Cost)

[Notes: Again this is an additional investment to reduce risk.]

Task 10: Complete final chip layout while the test chip is in fab and ready it for fab if all goes well with the evaluation of the test chip.

Time:	(Add for particular project)
Deliverables:	Final Chip Layout Database and verification results.
Investments:	(Add for particular project)

Task 11: Prepare evaluation and probe test methodology while test chip is in fab for both the test chip and the final chip. Make populated test boards.

Time:	(Add for particular project)
Deliverable:	Test chip/Final chip test flow document
Investment:	(Add for particular project)

This assumes that the customer will provide populated test boards for evaluation.

Task 12: Evaluate test chip after fabrication at both the customer's site and at SPG.

Time:	(Add for particular project)
Deliverables:	Evaluation results in documentary form.
Investments:	(Add for particular project)

[Note: This task would have to be done whether we do a test chip or not]

Task 13: Depending on the evaluation results of the test chip, modify the design of the final chip. [This step, may or may not be necessary, however we should keep this contingency in mind].

Time:	(Add for particular project)
Deliverables:	Layout database, verification results, schematics, simulation results.
Investments:	(Add for particular project)

Task 14: Final review of the chip after all modifications have been made. This will be the Critical Design review (CDR) face to face with all relevant data available, i.e. schematics, sim results, layout databases, test chip evaluation data, test flow and methodology. This review will decide whether the final chip will be released to fabrication or not.

At this point we will have to make a decision whether we will do automatic probe testing or not. If the volume of chips required is rather low it may be easier and (less costly to package the devices and test them on the bench at the customer site or at SPG. In any case this is a decision to be made. If the decision is to actually do probe testing we will have to start the test program activity right after CDR.

Task 15: Fabricate the final chip.

Time:	(Ad for particular project)
Deliverables:	10 to 20 engineering samples for evaluation
Investments:	(Add for particular project)

Task 16: Revaluate and fix. This milestone is difficult to estimate. In the best case there will be no need to go through this milestone if we do our jobs right at the test chip stage. However, if experience is a guide, we should plan for the contingency that something could still be in error and need fixing. In this case there will be some time set apart for fixing the design and a 2 to 3 mask fix in fabrication.

Time:	(Add for particualr project)
Deliverables:	Final samples
Investments:	(Add for particular project)

This ends the description of the program plan up to the development stage.

Options: It seems there are at least three options which can be considered in this development. These are as follows, with their attendant advantages and disadvantages.

Option 1: The first option is the costliest in terms of time and investment. If we chose this option the risk will be the lowest possible; we will develop a probe test program and of course a test chip to reduce risk. We will plan for contingency as well.

This option leads to the following times and investments.

O1: Design and Fab time to engineering samples including contingency and test program for automatic tester:

(Add for particular project) WW

Total Investment, includes design and development, fabrication, packaging etc.

(Add for particualr project)

Option 2: The second option is to leave out the automatic tester program and test the samples by hand since the volume is low but keep contingency and all the other items in option 1 above.

O2: Design and fab time to engineering samples, including packaging:

(Add for particlaur project)WW

Total investment, includes design and development, fabrication, packaging to engineering samples:

(Add for particlaur project)

Option 3: The third option is to do all the above in option 2, but not do a test chip and go directly to a full lot of production wafers:

O3: Total time to engineering samples: (Add for particular project) (includes contingency)

Total Investment to engineering samples: (Add for particualr project)

We believe these are the only realistic options open to us. In option 3, the lack of a test chip forces us to assume a higher risk therefore we must keep the contingency.

Financial Plan:

The total investment required for the successful completion of this project can be grossly divided into two sections. A design and development section and a manufacturing section. The design and development section is purely NRE while the manufacturing section is a mixture of NRE (labor and manufacturing expenses). The manufacturing expenses are composed of pure cost (amounts paid by us to the fabrication or manufacturing facilities) and some adders to accommodate the costs associated with managing the manufacturing interface. You may choose to do the manufacturing interfacing yourself in which case you could perhaps get a lower cost for manufacturing. However, in this case you would incur a higher management overhead. We leave the decision up to you. We are willing to work with either alternative.

For option 1, the manufacturing costs would be as follows: Test Chip fabrication, final chip fabrication, contingency fabrication, automatic test program and packaging. We will deliver about 25 working samples within the costs anticipated but further packaging will probably require further costs of packaging only. The rest of the investment is for development.

The total development investment would be: (Add for particular project)
The total manufacturing investment would be: (Addfor particular project)

We would like the following payment milestones for this option: (Each task has been defined in the above writeup)

1.0 Start of project: 20% of NRE

2.0 Definition: This task has been defined above .The expectation is that we will deliver a document that has been signed off by both the Telex team and the SPG team in roughly (Add for particular project).

Payment Milestone:

3.0 Technology Parameters and Design System Setup: This task has been defined in the writeup above. The expectation will be that in (Add for particular project), the technology parameters will be documented and delivered and that the design system will be set up and running so that all files included in the design setup will be delivered along with explanations of their significance and usage.

Payment Milestone:

4.0 Partition circuit and Mid point schematic and simulation results: These tasks have been described in the description above. The expectation is that we will deliver a document with block diagrams, interface specifications and all schematics and

simulation results to date at a mid point schematic review in (Add for particular project).

Payment milestone:

5.0 Design and Simulation of functional blocks complete. (Add for particular project)WW after the mid point schematic review we will deliver the complete set of schematics and simulation results in a documentary form as well as magnetic media. A review will be held to verify completion of this task..

Payment Milestone:

6.0 Top level chip simulations and schematics: (Add for particular project)WW after the functional blocks have been completely simulated we will complete the simulations and schematics of the major portions of the chip or as much can be simulated to verify performance of the complete chip. At the end of this time we will deliver all the schematics of the top level chip and simulation results of either the full chip or major portions as described above.

Payment milestone:

7.0 (Add for particualr project)WW after the final schematic review we will deliver the layout of all the functional blocks in a database format and color plots. This will complete the first phase of the layout task. All results of design rules checks, layout to schematic checks and explanantions of what we have done and its significance will be made available in a documentary form.

Payment milestone:

8.0 (Add for particular project)WW after the completion of the layout of functional blocks we will finish the layout of the test chip by interconnecting the functional blocks and any other test structures to form the complete test chip. We will deliver the layout database of the testchip, color plots and all other supporting documentation as above.

Payment Milestone:

9.0 Once agreement has been obtained on the test chip structure at a review we will send the test chip database to the foundry for fabrication. At this point we will require the payment of the fabrication costs for the test chip and packaging.

Payment milestone:

10.0 Complete the layout of the final chip while the test chip is in the fabrication facility. We will take (Add for particular project)WW to do this and the results will be a complete database of the final chip ready for fabrication if the test chip evaluation results are positive.

Payment Milestone:

11.0 After completing the final chip layout we will in (Add for particular project)WW work with the customer team to generate a test methodology for the test chip and the final chip. We will expect that the customer team will design and populate two test boards one of which will be given to the SPG team.

Payment milestone:

12.0 After the test chip completes fabrication, we will require (Add for particular project)WW to evaluate the test chip. This task will be done both by the SPG team and by the customer team. The results will be a determination of the functionality of the working parts of the chip and any other test structures that were put on the test chip. These results will be documented, delivered and reviewed. These results will predicate any further work on the final chip.

Payment Milestone:

13.0 Contingency: Depending on the evaluation results of the test chip we are assuming a contingency that further modifications on the final chip layout/design may be required. In this case we will take about (Add for particular project)WW to modify or update the design of the final chip. The results to be delivered are the final database of the chip along with a document outlining what changes were made and why and relating these changes to the results of the test chip evaluation. All supporting documentation consisting of DRC and LVS files and results, simulation results and final schematics will also be delivered.

Payment Milestone:

14.0 Automatic probe testing program generation. This task will be done if we want to test the wafers on an automatic probe tester. At this point we only have an estimate of what it might take. In any case it will take an estimated (Add for particular project)WW time to generate this program and we will also have to

make a probe card for the tester. I have estimated the total cost to be around $ (Add for particular project)

Payment Milestone:

Disclaimer: At this point in the program and financial plan the estimates for this milestone are only rough. These estimates can be fine tuned only after we (Customer team and SPG team) have completed task 11 in the program plan. Therefore this amount may increase or decrease.

15.0 Fabricate the final chip: We will send the database of the final chip to the foundry for fabrication. They will run further checks on the database to make sure we have not left anything out. After they finish running their checks they will send the database back to us. We will read the database back into our computers and run the same checks again just to make sure that no errors have crept in during transmission or the foundry checks. (This task is also done for the test chip). If no further errors are found then we will be ready to fabricate the final chip. Once the go ahead is given to the fab, they will invoice us for half the fabrication costs.

The usual terms are net 30. Therefore either you will have to pay them directly or if we are handling the manufacturing interface we will need this money. It takes about (Add for particular project)WW to get prototypes parts. Therefore the payment milestone for fabrication of the final chip will be split into two parts. The first payment milestone will be when the fabrication starts and the second will be when we receive the prototypes from the foundry.

Payment Milestone 1:
Payment Milestone 2:
Total:

These payments will be spaced about 8 WW apart.

16.0 Revaluate and fix the final chip. We are assuming that the first set of prototypes will have some kind of error in them. This is the contingency. The fact is if we have already gone through a test chip cycle there should either be no errors or very minor errors. This plan assumes that even if there are errors at this stage they will be minor, capable of being fixed with at the most 2 to 3 masks of fix and in a short time. Thus this milestone calls for testing the final chip and fixing any errors found and fabricating the chip again. We estimate (Add for particular project)WW for design fixes and (Add for particular project)WW for fabrication.

Payment Milestone: NRE
Fab

The deliverables will be 25 packaged samples of the product and at least 10 wafers. As more parts are needed we would package more parts. However, new

packages would require money for packaging which is not included in the above estimate. Since at this time the chip has not been completely defined it is difficult to estimate packaged parts. To provide an idea of packaging costs for low volumes, note that a 100 pin Quad Ceramic flat pack costs about $40.00 per package not including packaging labor. The lower the volume the higher the cost. Estimate at least $50 per package cost in a 100 pin package if we buy 10 or 20 packages. It may be much lower for higher volumes such as a 1000 parts. Again it appears useless to speculate on exact numbers until we a good definition of the chip.

This ends the description of the financial plan numbers. Note that there are at least three options which have been described above. To get numbers for the other options it should be relatively simple to delete entries in the plan for the options that are being considered . Obviously the plan described above is the worst case in terms of investment and time but the best case for risk. Other options will trade off these three issues.

Invoicing and Payment terms for SPG: We will invoice as shown above in the financial plan. Our standard terms are payment on receipt of all invoices. Delayed payments will incur penalties if we have done the job on time we expect to be paid on time. Delayed payments lead to untold problems for us and the work gets effected to the point that we will become totally ineffective as contributors to the project.

Changes to project scope: We have no problems about changing the scope of the project as long as we get to quote on the revised project. If changes are so minor that they will not effect the progress of the project then there is no need of any *ECR's but major changes will require an ECR with its associated changes in investment and time.

*ECR = Engineering Change Request.

Ownership: The customer will own all rights to the chip.

Confidentiality: All materials given to us by the customer will be considered confidential and proprietary and not to be shared with any third parties except on a "Need to Know" basis.