

# Basic concepts in RF power amplifier design – Load line analysis and conclusions

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- I. A good place to start with understanding RF power amplifier design is to understand the graphs shown below in Figure 1.0

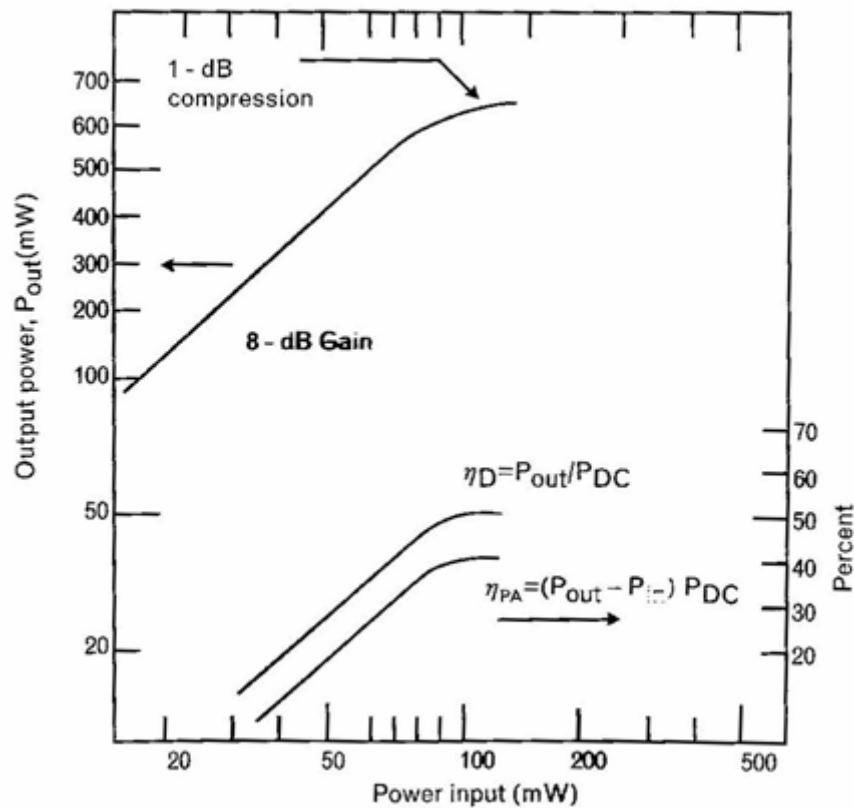


Figure 1.0

The following definitions can be enunciated:

- I1.0 **1 dB compression point:** As the input power to a power amplifier is increased the output power increases *linearly to a point*.

However as the input power is further increased the output no longer follows but starts reducing. When the output power falls to one dB below the extrapolated linear range of output power, the 1 dB output compression point has been reached. This is an important specification for a RF PA. This point is graphically illustrated in Figure 1.0 ( upper trace).

**II.0 Efficiencies:** The lower traces on the right hand side of Figure 1.0 show the other very important figures of merit for a RF PA ( or indeed, any PA). These are the efficiencies.

The drain or collector efficiency is simply the ratio of RF power to dc input power,

$$\text{eff}_D = \text{POUT}/\text{PDC} \quad (1)$$

where POUT is the RF power and PDC is dc input power.

Another more revealing figure of merit is the “power-added” efficiency defined by,

$$\text{eff}_{\text{PAD}} = (\text{POUT} - \text{PIN})/\text{PDC} \quad (2)$$

where PIN is the input RF power, POUT is the output RF power and PDC is the dc input power.

Power added efficiency measures the incremental RF power added by the device, comparing the output power to the level of input power needed to achieve it.

This measure of efficiency depends on the gain of the device, since  $\text{POUT} = G \cdot \text{PIN}$ .

**II.0 The load line:** A useful and important tool in RF PA design is the load line. This is explained below. Consider Figure 2.0

below of a typical PA with an inductive load. A very common circuit.

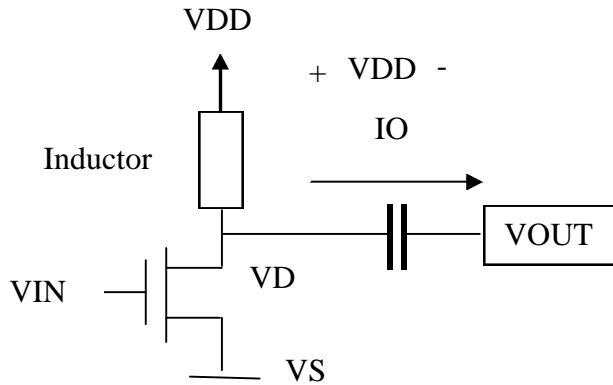


Figure 2.0

The fundamental equations are:

$$V_{DS} = V_{DD} + V_O \quad (3)$$

$$I_Q = I_D + I_O \quad (4)$$

$I_Q$  is the quiescent current. The other quantities are indicated Figure 2.0.

If we constrain the output voltage and current through the load impedance :

$$Z_L = V_O / I_O \quad (5)$$

The from equation (3) and (4),

$$I_D = I_Q - (V_{DS} - V_{DD}) / Z_L \quad (6)$$

Equation (6) defines how the transistor output current changes with voltage  $V_{DS}$ .

The trajectory defined by equation (6) is called the load line.

Figure 3.0 below shows the results graphically for various conditions.

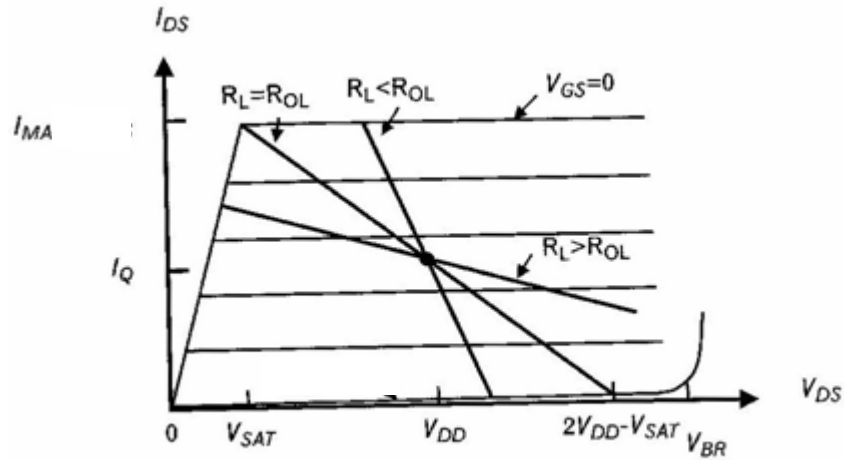


Figure 3.0

The transistor VDS is assumed to switch between  $2V_{DD} - V_{SAT}$  and  $V_{SAT}$  and  $I_{DS}$  switches from some value  $I_{MAX}$  and approximately 0.

The quiescent current is assumed to be  $\frac{1}{2} (I_{MAX})$  to allow symmetrical switching.

The nominal load resistance is defined as  $R_{OL}$  and its slope varies.  $R_{OL}$  is defined by,

$$R_{OL} = (2V_{DD} - V_{SAT})/I_{MAX} \quad (7)$$

The nominal resistance is  $R_{OL}$ . The figure also shows what happens when the load resistance  $R_L$  value is above or below the nominal  $R_{OL}$  value.

The slope of the load line changes as shown. A little elaboration is required to explain the load line .

As the input voltage ( gate voltage ) of the MOSFET changes the output current and voltage swing on the load line. The RF choke ( inductor) permits the maximum output voltage to swing symmetrically by almost 2VDD. ( This amplifier is a Class A power amplifier for purposes of explanation).

As can be seen from the expression for ROL, the optimum load resistance is a function of two parameters. The bias point and the set of MOSFET ( or other active device) parameters.

It is immediately apparent that if VSAT is very low, then ROL is very high. Also if VDD is increased then ROL is increased for the same IMAX.

Now, for power amplifiers the devices used are higher current devices. So if VSAT is the same and VDD is the same, *ROL will decrease significantly.*

As the devices get larger the optimum load resistance becomes excruciatingly small. Therefore matching the output impedance becomes a problem. To offset this problem VDD is usually increased whenever possible.

The power into the load is:

$$PRF = (I_{PEAK} * V_{PEAK}) / 2 = I_{MAX} (V_{DD} - V_{SAT}) / 4 \quad (8)$$

Therefore it is apparent from this equation that maximum power is delivered when the a maximum current swing *and* a maximum voltage swing is generated *in phase.*

The load line imposes the constraints that the maximum voltage swing goes from the knee of the device curve to its breakdown, i.e VBR.

The maximum current swing is limited to the peak to peak value of the current IMAX.

In this case the maximum power available from the device is:

$$P_{MAX} = I_{MAX}(V_{BR}-V_{SAT})/8.0 \quad (9)$$

This power will be obtained when the bias voltage is set to:

$$V_{DD} = (V_{BR} + V_{SAT})/2.0 \text{ for symmetrical swings.}$$

If the value of  $V_{DD}$  in (8) is replaced by this expression, the result is equation (9).

Obviously we are not always free to choose  $V_{DD}$ .  $V_{DD}$  may have various constraints on it too, like battery voltages and so on.

To achieve the best power condition we need to use the optimum load resistance value of  $ROL$ .

We must remember that for maximum power the current and voltage of the internal device must be in phase and at their maximum swings. The output matching network must null out any load mismatches and any reactive parasitic components .

In Figure 3.0 the effects of  $RL < ROL$  and  $RL > ROL$  are also shown. Note from the figure that when the load resistor is too small ( compared to  $ROL$ ), the output voltage swing will be smaller. This circuit is a current limited design since the maximum current determines the power output.

Conversely when  $RL > ROL$  then the current cannot swing to the maximum extents. In this case we have a voltage limited power amplifier, since the output power becomes limited by the voltage swing.

Distortion: The load line is also very useful in determining when distortion may set in. With reference to Figure 4.0, note that as long as the current swings within the linearly spaced transistor characteristics, the distortion in the output waveform is minimal. However, note that the characteristics at the two extremes are no longer linear but bunched up. When the input drive is such that the input signal drives to these limits

the output waveform becomes distorted leading to third order distortion products.

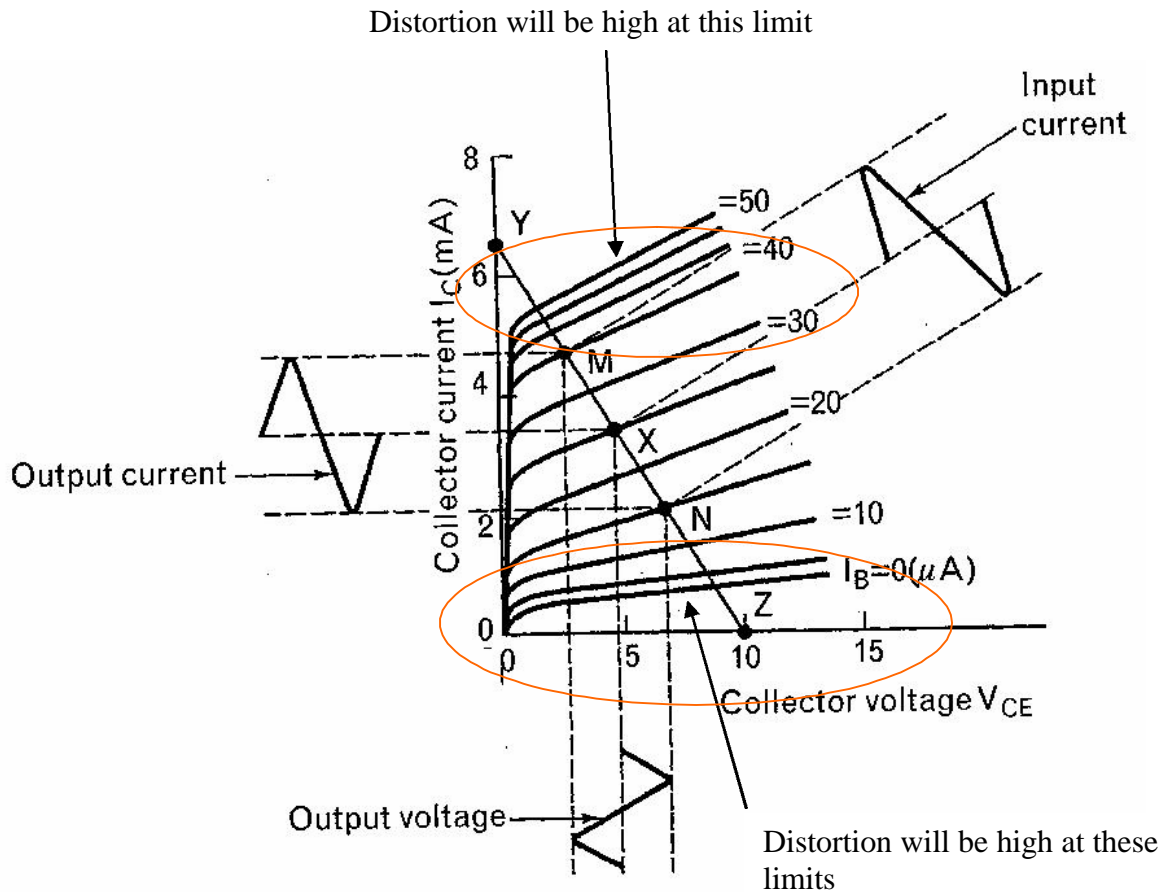


Figure 4.0

Other considerations: A few other issues are discussed here.

(1) Reactive loads: If the load contains reactance then  $Z_L$  will not be a real number. The current and voltage will no longer be in phase. The load line then will become an ellipse around the bias point.

Obviously the ratio of the two axes will be proportional to the load.

(2) Drain ( or collector) bias voltage: The basic assumption that was made in earlier considerations was that the DC resistance of the inductor was zero. This is usually not the case and some finite resistance will be present in the inductive load. This will change the slope of the load line. The effect of this additional resistance then must be taken into account.

- (3) Harmonics: Harmonics in the waveform will also change what the load line looks like. Harmonics can change the movement of the current and voltage along the load line. In the extreme case the movement may stop altogether ( in case of a square topped or bottom waveform).
- (4) Parasitics: Package or other parasitics play a significant role in power output. For example the package parasitics can form ( and usually do) a low pass filter with a corner frequency that is way beyond the frequency of operation of the circuit. Beyond those limits it will be very difficult to get power out of the device.
- (5) High power versus high gain: We cannot assume our DC analysis using the load line is valid at RF. Therefore if the device has a variation in its intrinsic parametrics ( such as the output resistance or capacitance), then the performance of the amplifier will be affected. At this point it becomes difficult to use the load line as a definitive measure of RF performance. However, the load line is used to derive an optimum load resistor for maximum output power.

When the amplifier is operating in a small signal regime, the small signal output resistance is greater than the optimum load. This leads to higher power output at small signal levels from the small signal output resistor. So to transfer maximum power at small signal levels the output resistor will also be the same value.

For large signals and at high power levels the output power and the large signal gain will be higher.

Conclusions: A brief expose of load line effects has been outlined above. A load line is a great tool for power evaluations, distortion and large signal gain estimates. It provides a graphical method of visualizing the operation of a power amplifier and allows quick evaluation of devices which may or may not be suitable for a particular power stage.

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