Typical Starting Points and Methodologies for Full Custom Analog Integrated Circuits and Micro-Systems Development and Manufacture. By SPG Staff.

Introduction: The following scenarios are typical, when it comes to thinking about developing a full custom integrated circuit. Each scenario has its own roadmap when it comes to developing a low risk, highly successful chip. This brief article explores the possibilities for embarking on and finally delivering on the promise of a fully integrated solution. Note that these descriptions are for analog/RF and MMIC or analog-digital integrated circuits and micro-systems. Purely digital chips have a different methodology.

Typical scenarios could be:

1.0 **A new concept** has been enunciated but no clear-cut approach has been developed,and no specifications are available. The product will have to be based on custom integrated ICs to really deliver on its potential. However, either enough in - house knowledge about the integration process is not available or a lot of work will have to be done on the concept before a clearcut approach to development of the custom chips emerges.

2.0 **A breadboard is available, and works**. There are a lot of wires and interconnects with a large numer of discrete packages of various types. It has to be integrated to realise its true potential. Otherwise the huge number of interconnects and mulitple packages will make the assembly clumsy and costly to produce. There is significant analog content on the prototype board. Noise and crosstalk is a problem from long inductive leads and mutual coupling among other things.

3.0 **A working product built from discrete components on a PCB, is selling in the market**.

Volumes have risen to a level that justify a cost reduction by integration or that volumes of product can be increased if the product can be cost reduced or both. It will take too much effort in house to really work on setting up specifications and writing descriptions of the requirements, getting other documentation to transfer the knowledge to someone who could work on the cost reduction. However, the schematics of the board level product and test results on it are available. Again there is significant analog content on the board and product.

4.0 **An IC that is being used presently in the product has been discontinued by the supplier.**

A last time buy has been made but more of the same device will be required. It has been found after enquiries a close fit cannot be found with existing technology and changes will have to be made either to the design of the device, or technology will have to be found which can accomodate the requirements of the device. The required technology cannot be found in standard offerings. In the absence of these options a complete redesign of the product will have to be done which will cost money and time to complete and qualify or that the product itself will have to be discontinued!

5.0 **A new concept has been breadboarded and a specification exists.** In order to package the product, *size must be reduced* by integration. However, the product design contains functions that cannot be easily integrated in standard processes. For example, a low voltage function in association with a high voltage - high current function, or a low noise functional block in the proximity of fast edges or high frequency functions (wireless), combined with audio functions, combined with a microcontroller and digital logic. A voltage inverter to boost voltage and power etc. A real system on a chip in fact. Again there is significant analog content on board which will be affected.

6.0 **A working prototype is available but consumes too much power** because of the use of standard parts that are not customized for use in the application. e.g. a bigger memory than is required etc. Use of standard parts with duplicate functions which will actually have to be turned off or other standard packages whose full functionality is not being used. Integration in a custom device will reduce the power thereby allowing the product to become more attractive and meet market demand. Again the product has significant analog content or it is the analog content that is causing the problem!

7.0 **A prototype has been built but has to be operated at lower levels of performance** because of the increased parasitics on a pcb. Enhancements in performance can only come by reducing the number of interconnects, reducing lead lengths, reducing parasitic capacitances and inductances. A standard part or parts are just not available to do the job and the prototype actually uses a completely discrete design which may have to be repeated multiple times to achieve the functionality. The size of the discrete designs is such that it acts to increase size and parasitics thereby compounding the problem. In short, a point of diminishing returns has been reached and there is nothing for it but to develop a custom analog - digital IC.

These are just a few of the typical issues have to faced by a design and development team when you start considering a custom IC. Questions are :

How do I get started if I want to use the technology?
What are the ways to interface to a custom IC development and manufacturing house?
What kind of documentation will be required?

For answers to the above three questions see the document, “Doing business with SPG” on the website at www.signalpro.biz.

Who will develop this information?

Typically the required information is developed by members of the SPG TechTeam and the customer.

What are the risks?

Risks are very low if the SPG standard operating procedures are followed. SPG espouses Risk Reduction as a primary metric of its operations.

How long does it take?

There is no typical time line. A range would be anywhere from 12 weeks to 18 months depending on the complexity of the device.

How much money will it cost?

Again there is no standard price line. The investment is directly proportional to the complexity of the device. A range would be from $25,000.00 to $300,000.00 in a majority of cases.

Can technology be customized to my requirements?

Definitely. However, in this case a technology development fee would be charged by our fabrication partners ranging anywhere from $5,000.00 to $50,000.00 depending on the type of modifications or development.

What responsibility do I have to take in the overall process?

The usual case is in supporting the development of specifications, be avaliable for preliminary and critical design reviews and support for the system side of the project.

What are the different steps required to develop a succesful Analog or Analog - Digital IC from where I am now?

Specifications, system and behavioral models, schematics and simulations, layout and layout verification, fabrication, testing and packaging.

What can be integrated and what cannot be integrated?

Active devices can be integrated, low value passive devices (Resitance < 50 Meg and Capacitance < 1nF) can be integrated, inductors (< 1uh). Again there is much dependence on the size (and therefore of the cost) of the device.

What external components will be required even if a significant portion can be integrated?

Typically, large bypass capacitors, large inductors.

What are the parameters of design anyway?

Fundamental parameters are supply voltages, supply currents, operating and maximum temperatures, digital delay times, matching accuracies of devices such as offsets and. frequency response and output current drive/voltage swings.

What kind of environmental factors will I need to take into account?

Generally temperature, humidity, mechanical and vibrational.

How should I conduct reviews once I decide to use someone to build a custom IC for me?

Have a kickoff review, a preliminary design review (schematics and simulations), a crtical design review (layout and layout verification), test and packaging reviews.

What kind of deliverables should I ask for and what is standard in the industry?

Schematics and layout databases in GDS 2 format. Bonding diagrams. Test log files. PCM data from the fabricator.

What options do I have in my requirements, low cost, low volumes or other?

Low volume (< 100 units), also implies low cost sometimes for the development devices.
High volume is standard. A mixture of the two. Low volume low cost development devices to try out the technology followed by high volume production.

What does low cost imply?

Anywhere from $25,000.00 to $35000.00 for development fabrication. $10,000.00 to $35000.00 for development design engineering.

What does low volumes mean?

10 units to 1000 units

Can I get second sourcing?

Yes. Second sourcing is usually available.

Who will own the design?

The customer owns the design if he/she pays for it. SPG owns the IP to the functional blocks.

What kind of financing options are available?

If committed volumes a very high (i.e we are able to recover our costs plus a small profit within a year) NRE can be shared with the customer.

What is a small chip? A large chip?

A small chip is somewhere around 15 mil –75 mil on a side. A large chip is 200 mil on a side and above

What do the various buzzwords in semiconductors actually mean?

A glossary will be available shortly.

Will the new technology I am using today be obsoleted? What can I do about this?

Technologies do get obsoleted. However the lifetime of a technology is usually 10 years or more. Last time buys are available from the fabricator and SPG's obsoleted device service can provide new devices on demand.

What are the latest trends in semiconductor technologies?

CMOS technology is moving toward 45nm sizes and less. High frequency technologies such as SiGe and GaAs are being used more frequently. More and more passive elements can now be implemented on chip in addition to the active devices.

Can I buy a standard product and customize it to my use?

Yes.

What reasonable guarantees can I ask for?

That your production devices will have a very low failure rate. This rate is agreed to in advance with SPG using the supplier agreement. That all reasonable precautions will be taken to reduce risk in the design.

What happens if there is a problem in the design or manufacture? Who is responsible?

If the specification has been agreed to with a customer and accepted by SPG, SPG is responsible. If the customer makes changes (“mission creep”) then the responsibility is jointly shared. To avoid this a SPB ECR shoul dbe used by the customer.

What are test flows for ICs?

There are usually three major types: (1) DC tests (2) AC and transient tests (3) Stress tests.

What kinds of tests are performed?

The first time test is a comprehensive test which exercises the complete device function in all facets of operation. Subsequent to this the number of tests may be reduced to reduce test time if it is ascertained that these tests are not critical or have very low probability of failure. Some agencies (particularly the military , medical or auomotive) may still stick to the comprehensive test throughiout.

These and a few other questions are all reasonable and rational and must be asked. This article has attempted to answer as many as possible through a structured approach of descriptions of tasks in the development and manufacture of full custom Analog and Analog - Digital ICs. We request that any additional questions generated be added to this list so more answers and FAQs can be forthcoming.
